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A lamp thermoelectricity based integrated bake/chill system for photoresist processing

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Abstract

The design of an integrated bake/chill module for photoresist processing in microlithography is presented, with an emphasis on the substrate spatial and temporal temperature uniformity. The system consists of multiple radiant heating zones for heating the substrate, coupled with an array of thermoelectric devices which provide real-time dynamic and spatial control of the substrate temperature. The integration of the bake and chill steps eliminates the loss of temperature control encountered during the mechanical transfer from the bake to chill step. The feasibility of the proposed approach is demonstrated via detailed modeling and simulations based on first principle heat transfer analysis.

Keywords: Microlithography; Photoresist processing; Temperature control; Lamp heating; Thermoelectricity

1. Introduction

The lithography process is the most critical step in the fabrication of nanostructures, accounting for one-third of the costs of integrated circuit manufacturing. Thermal processing of semiconductor substrates through conductive heat transfer is common and critical to the lithography process [1]. Each thermal processing step involves baking the substrate to an elevated temperature for a given period of time, this is then usually followed by a chill step which is used to cool the wafer to an appropriate temperature for subsequent processing [1]. Of these baking steps, the post-exposure bake step is the most sensitive to temperature variation for the current generation of chemically amplified resists (CARs) [2]. For such CARs, the temperature of the wafer during this thermal cycle has to be controlled to a high degree of precision both spatially and temporally [3,4]. For example, Sturtevant et al. [3] reported a 9% variation in the linewidth or critical dimension (CD) per 1% variation in temperature for a deep ultraviolet (DUV) resist. A number of recent investigations also show the importance of proper bakeplate operation on CD control [5,6].

According to the International Technology Roadmap for Semiconductors [7], the post-exposure bake (PEB) resist sensitivity to temperature will be ever more stringent for each new lithography generation [2]. With a precise temperature control, existing resists can be used for future technology nodes. Although less temperature sensitive photoresist materials are desired, the requirements become more stringent as the feature size shrinks. Consequently, the temperature control system for this process requires careful consideration, including the equipment design and temperature sensing techniques. The application of mathematical systems science tools have seen increasing utilization in recent years to improve yields, throughput, and in some cases, to enable the actual process to print smaller devices [8,9].

In the thermal processing of semiconductor substrate during lithography, the heated plate is usually thermally

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massive relative to the substrate (e.g. silicon wafer) and is held at a constant temperature by a feedback controller that adjusts the resistive heater power in response to a temperature sensor embedded in the plate near the surface. Because of its large thermal mass and resultant sluggish dynamics, conventional hotplates are robust to large temperature fluctuations and loading effects, and demonstrate good long-term stability. These advantages however become shortcomings in terms of process control and achievable performance when tight tolerances must be maintained. Other disadvantages include uncontrolled and non-uniform temperature fluctuation during the mechanical transfer of the substrate from bake to chill plates, spatial temperature non-uniformities during the entire thermal cycle, etc. [9,10]. This lack of a method to conduct real-time distributed, closed-loop temperature control with conventional hotplates is a source of process error in the lithography chain.

In this paper, we describe a new thermal processing system developed for optimal processing of temperature sensitive photoresist so as to address the above-mentioned issues. This development is motivated by the general inclination to improve the capabilities of conventional hotplates through advanced control algorithms alone. Although some improvements are possible [11,12], we conclude that the conventional hotplate design has poor controllability [13] that ultimately limits the achievable performance. Our proposed system comprises multiple radiant heating zones for heating the substrate, coupled with an array of thermoelectric devices (TEDs) which provide spatial and temporal temperature uniformity control and active cooling. The proposed system offers excellent temperature control during the entire thermal cycle, eliminates substrate movement during the baking and chilling processes, and accommodates in situ temperature measurement for real-time control. The feasibility of the proposed approach is demonstrated via detailed simulations based on first principle heat transfer modeling. Other unique applications are rendered possible because of the rapid response, and real-time sensing capabilities exhibited by this thermal processing technology. For example, our method offers an elegant solution to the bake–chill transition in an oxygen free environment commonly encountered in copper annealing. Other demanding applications include thermal control of spin-on dielectrics or low-k materials.

2. Proposed thermal processing module

Efforts in addressing some of these issues have been ongoing by our collaborators and us [14–18]. A fluid-heat-exchanger based thermal cycling module was developed earlier [14,15]. The heat-exchanger module provides thermal cycling by alternating between hot and cold fluids. Spatial and temporal control were provided by auxiliary heaters in the form of thermoelectric devices [14] and a multizone etched foil heater [15]. Both methods, while having a much lower "thermal mass" than conventional units, still require large amounts of power for thermal cycling. The use of fluids for bulk heating is costly, and the presence of hot fluids in the system represents a safety hazard. The etched foil heater units also deflect during cyclings and thus raising the concern regarding long-term reliability. A considerable improvement was achieved in a spatially programmable module using an array of cartridge heaters developed by Kailath's group in Stanford [16,17] and subsequently commercialized. This system is excellent for processing substrates but without modification, it may not be able to achieve fast enough ramp-down rates during a thermal cycling operation. In addition, all of the above approaches lack the capability to conduct real-time temperature control on the substrate. A notable exception is our recent work [18] featuring a thermal cycling module integrated with in situ measurement of substrate temperature.

Because resist processing steps are thermally activated, a performance specification is required to take into account non-uniformities during the transient and steady state [10]. This indicates that the ability to create any arbitrary temperature profile is highly desirable and one approach is to have a system that can provide extremely fast ramp-up and ramp-down rates. One attractive solution is the use of a lamp based heating method which is common in rapid thermal processing (RTP). In RTP, intense radiation is used to heat the wafer to temperatures over 700 °C for annealing and oxidizing the wafer. As in photoresist processing, it is important in RTP to maintain temperature uniformity, although the temperature requirement is not as stringent as in photoresist processing. In RTP, active cooling is usually not available, chilling is typically achieved by turning off the lamps. In this paper, we propose to make use of this radiant heating technology coupled with TEDs to provide for both active heating and cooling. The proposed method for photoresist processing will also be suitable for low-temperature RTP processes. Constructing such a prototype would be cost-prohibitive as energetic efficiency mandates a gold-coated chamber; instead we present a detailed simulation of the system based on first principle thermal modeling.

A schematic of the proposed thermal processing module is shown in Fig. 1. The system consists of a heating chamber with three annuli of tungsten halogen lamp arrays. Energy is radiated through a quartz window of the lamps onto a semiconductor substrate either directly or via reflections from the chamber walls. This lamp structure design is an offshoot of the Stanford RTP system design [26,27]. The power ratings of lamps are kept sufficiently high to prevent saturation during the thermal cycle. The exact capacities of the lamps will depend on the configuration of the lamp structure/placement. To achieve optimal temperature uniformity, the output heat flux profile of each zone can be optimized based on the lamp positions and size. Suitable filters are used to prevent the photoresist from being exposed to UV irradiation during the post-exposure bake step in lithography.

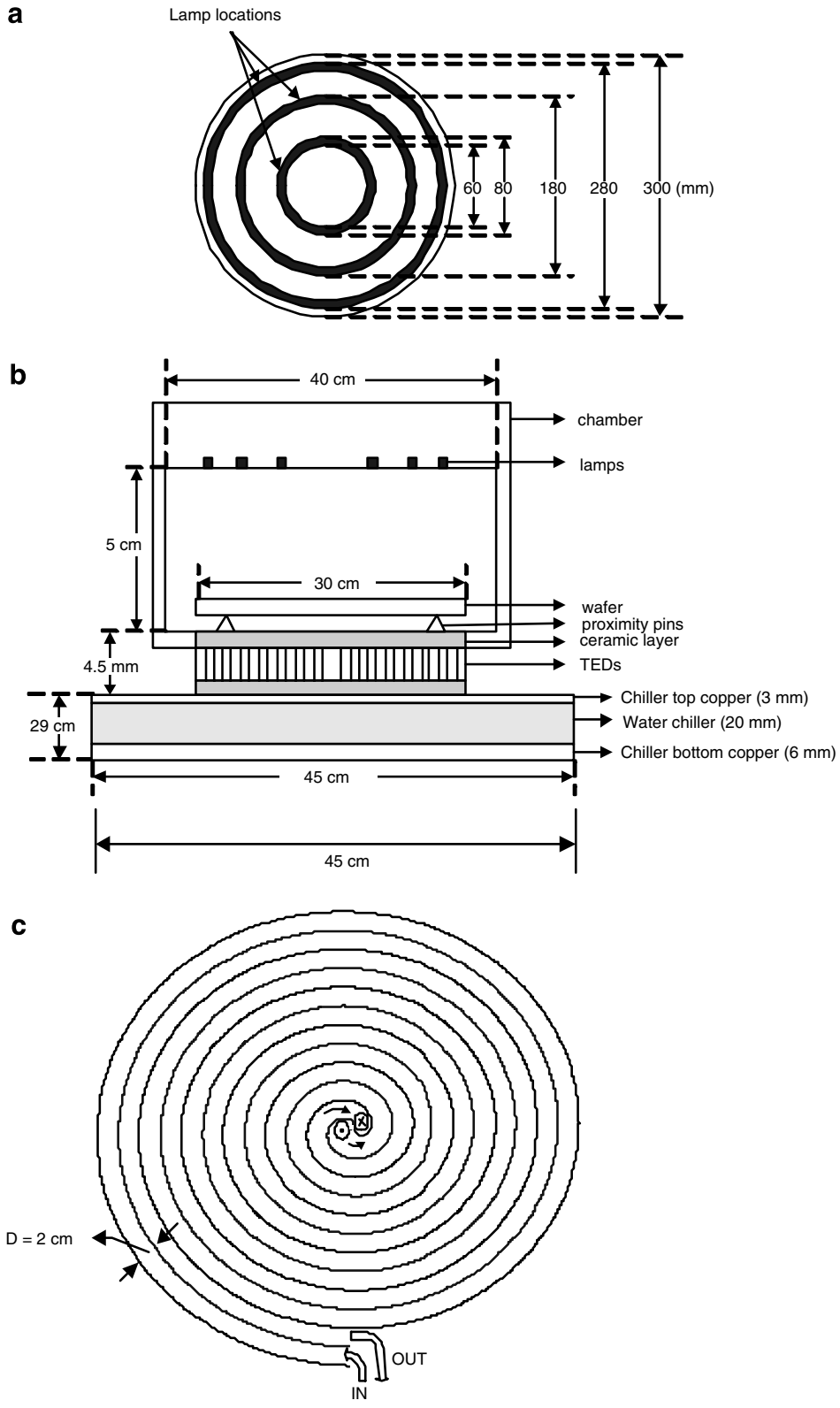

Fig. 1. Schematic diagram of the integrated bake/chill design. (*Note:* Figure not drawn to scale.)

The substrate sits on an array of proximity pins approximately 5 mils above the ceramic. These proximity pins can be embedded with temperature sensors [28] (with an accuracy of ±0.5 °C and 25 ms response time) to provide in situ temperature measurement. Proximity baking is the preferred method in the industry compared to contact baking

due to contamination issues. The bismuth telluride thermoelectric devices (TED's) provide real-time dynamic and spatial control of the substrate temperature. The TEDs sit on top of a chiller (see Fig. 1(c)) and together form the cooling mechanism. The TEDs are assembled such that they can be controlled independently as separate annular zones. Annular TEDs, although not common, can be custom made [29].

A typical heat-and-chill cycle would proceed as follows. The whole system, with the substrate sitting inside, starts at around room temperature. During the baking process, the lamps will be switched on and progressively heat up the wafer. The gold-coated chamber, characterized with a very low emissivity facilitates the heating up of the wafer. During the baking process, the various zones of TEDs will be separately and judiciously energized to maintain temperature uniformity throughout the wafer. Depending on the polarities applied to the TEDs, they can operate in either heating or cooling mode. This makes them excellent regulating devices. Chilling is achieved by switching off the lamps and dictating the TEDs to provide active cooling and maintaining temperature uniformity. The chiller unit consisting of cold circulating water (or fluid) serves as the dominant means for heat transfer. As shown in Fig. 1(c), the chiller is designed to provide uniform temperature across the chiller surface.

3. Thermal modeling

In order to ascertain the performance of the proposed design, a mathematical model is developed for the integrated bake/chill operation. We assume that the substrate is a silicon wafer and adopt an axisymmetrical cylindrical coordinate system. Fig. 1 presents the three main sections of the system: viz. the annular lamp arrays, wafer, TEDs and heat sink. We will subsequently consider the complete optical properties of a silicon wafer and the governing equations for the major system components.

3.1. Lamp design considerations

The lamp system consists of three annuli lamps arrays as shown in Fig. 1. The encapsulation of the tungsten filaments by a quartz envelope dictates that no radiation beyond 4 μm [20] wavelength from the filament will be transmitted through the envelope. In addition, we employ a typical glass filter [21] to prevent resist exposure to wavelengths below 500 nm. A host of glass filters with different cutoff wavelengths [21] is available to cater to most types of photoresist.

Since it takes a finite time to heat up the tungsten filaments, the thermal mass of these lamps have to be considered. Our quartz tungsten halogen lamps are from Oriel Model No. 6337 [22]. Based on the data sheet provided therefrom, the thermal mass of each of the annular lamp arrays is computed and tabulated in Table 1.

3.2. Thermal radiative properties of silicon wafer

We consider the chamber walls to be diffuse, opaque and gray and the lamp zones gray and Lambertian. For our temperature regime, the silicon wafer is translucent [19], so that its various spectral optical properties have to be taken into account. The range of wavelengths between 500 nm and 4 μm sufficiently encompasses the domain of radiative interaction of our application. The spectral emissivity, ϵ_λ, of silicon wafer can be computed as follows [23,24].

$$\epsilon_\lambda = \frac{(1-R_\lambda)(1-T_\lambda)}{1-R_\lambda T_\lambda} \tag{1}$$

$$R_\lambda = \frac{(n_{\mathrm{si},\lambda}-n_{\mathrm{air}})^2 + k_{\mathrm{si},\lambda}^2}{(n_{\mathrm{si},\lambda}+n_{\mathrm{air}})^2 + k_{\mathrm{si},\lambda}^2} \tag{2}$$

$$T_\lambda = \exp(-\kappa_\lambda z) \tag{3}$$

$$\kappa_\lambda = \frac{4\pi k_{\mathrm{si},\lambda}}{\lambda} \tag{4}$$

The silicon spectral absorption coefficient, κ_λ, and refractive index, n, can in turn be computed as a function of wavelength and temperature [24]. For photoresist processing, the wafer is usually at a processing temperature of about 100 °C [2] most of the time. As such, all computation of the various optical properties are done at 100 °C. Fig. 2 shows the spectral emissivity for a standard 300 mm wafer of thickness 675 μm; the emissivity is essentially zero after 1.3 μm.

In addition to the spectral emissivity, the apparent reflectivity, ρ_λ, and transmissivity, τ_λ, are also important for the computation of the various surface radiosities in the system. The apparent reflectivity and transmissivity consider reflections from both the top and bottom surfaces of the wafer and treat them as effective surface phenomena. Invoking the Kirchhoff's law [23], the following relationship holds:

$$\epsilon_\lambda + \rho_\lambda + \tau_\lambda = 1$$

where

$$\rho_\lambda = R_\lambda\left[1 + \frac{T_\lambda^2(1-R_\lambda)^2}{1-R_\lambda^2 T_\lambda^2}\right], \quad \tau_\lambda = T_\lambda\frac{(1-R_\lambda)^2}{1-R_\lambda^2 T_\lambda^2}.$$

The apparent reflectivity and transmissivity are also shown in Fig. 2.

3.3. Heat transfer in wafer

The wafer is assumed to be cylindrical with a diameter D, thickness Z and negligible thermal expansivity. The wafer temperature is also assumed to be uniform in the axial z direction as the wafer is thin. The wafer is

Table 1
Physical parameters of the thermal processing system [31,37]

	Property	Value
Lamp	Emissivity, ϵ	0.425
	Thermal mass of zones 1, 2, 3	0.0041 kg, 0.0099 kg, 0.0157 kg
Chamber (unpolished gold coated)	Emissivity, ϵ	0.02
	Density, ρ	8933 kg m^{-3}
	Specific heat capacity, c_p	385 J K^{-1} kg^{-1}
	Thermal conductivity, k	401 W m^{-1} K^{-1}
	Thickness, t_{ch}	1 mm
Wafer (silicon)	Density, ρ	2330 kg m^{-3}
	Specific heat capacity, c_p	712 J K^{-1} kg^{-1}
	Thermal conductivity, k	148 W m^{-1} K^{-1}
	Thickness, Z	0.675 mm
	Diameter, D	300 mm
Ceramic	Emissivity, ϵ	0.9
	Density, ρ	3110 kg m^{-3}
	Specific heat capacity, c_p	375 J K^{-1} kg^{-1}
	Thermal conductivity, k	36 W m^{-1} K^{-1}
	Thickness, t_c	0.5 mm
Metal contact (copper)	Density, ρ	8933 kg m^{-3}
	Specific heat capacity, c_p	385 J K^{-1} kg^{-1}
	Thermal conductivity, k	401 W m^{-1} K^{-1}
	Thickness, t_m	0.25 mm
Thermoelectric elements[a]	Density, ρ	7534 kg m^{-3}
	Specific heat capacity, c_p	554 J K^{-1} kg^{-1}
	Thermal conductivity, k	1.5 W m^{-1} K^{-1}
	Seebeck coefficient, α	$(22224 + 930T - 0.9905T^2) \times 10^{-9}$ V K^{-1}
	Electrical resistivity, R	$(5112 + 163.4T + 0.6279T^2) \times 10^{-10}$ Ω m
	Thickness, t_{TED}	3 mm
Air in chamber	Density, ρ	1.239 kg m^{-3}
	Specific heat capacity, c_p	1000 J K^{-1} kg^{-1}
	Thermal conductivity, k	0.025 W m^{-1} K^{-1}
Chiller (copper)	Density, ρ	8933 kg m^{-3}
	Specific heat capacity, c_p	385 J K^{-1} kg^{-1}
	Thermal conductivity, k	401 W m^{-1} K^{-1}

[a] In the computation of the Seebeck coefficient, α, and electrical resistivity, R, the temperature, T, is the average temperature of the hot and cold junction of the TED [38].

discretized and for each discrete wafer element, the following diffusion equation holds.

$$\dot{T}_i = \frac{1}{\rho v_i c_p}\left(\frac{k v_i}{r}\frac{\partial}{\partial r}\left(r\frac{\partial T_i}{\partial r}\right) + q_i\right) \tag{5}$$

where q_i the net heat input per unit volume into each wafer element embodying radiative and convective losses from the wafer element, radiative absorption by the wafer element and conductive heat transfer from the TEDs.

A finite difference scheme is employed for our numerical computation. The wafer is discretized into 15 zones (1 circular and 14 annular elements). The edge of the wafer is taken into account when we compute for the radiative interaction. The TEDs will also be arranged into 15 zones similar to the wafer. Such circular and annular TEDs can be custom made [29]. For the same purpose, the chamber ceiling is divided into 20 zones comprising one circular zone and 19 annular zones. Some of these zones are used to represent the annular lamp arrays. The outer radius of each zone increases uniformly from the center zone to the edge zone. The portion of the chamber sidewall between the wafer bottom surface and the chamber ceiling is divided into five equal zones. The annular region between the wafer bottom surface and the chamber bottom surface is treated as one zone. The remaining floor of the chamber (including the ceramic surface of the TEDs) is divided into 20 zones corresponding to the ceiling. The radii of the annuli increase uniformly from the center zone to the edge zone. The system dimensions are shown in Fig. 1.

The net heat transfer q_i into each wafer element i is taken as the sum of the following terms:

$$q_i = q_i^{em} + q_i^{abs} + q_i^{cond} + q_i^{conv} \tag{6}$$

with each term explained below.

(1) Radiation emitted by wafer element i, q_i^{em}:
The radiation emitted by hot objects has a spectral distribution related to the Planck's distribution [25].

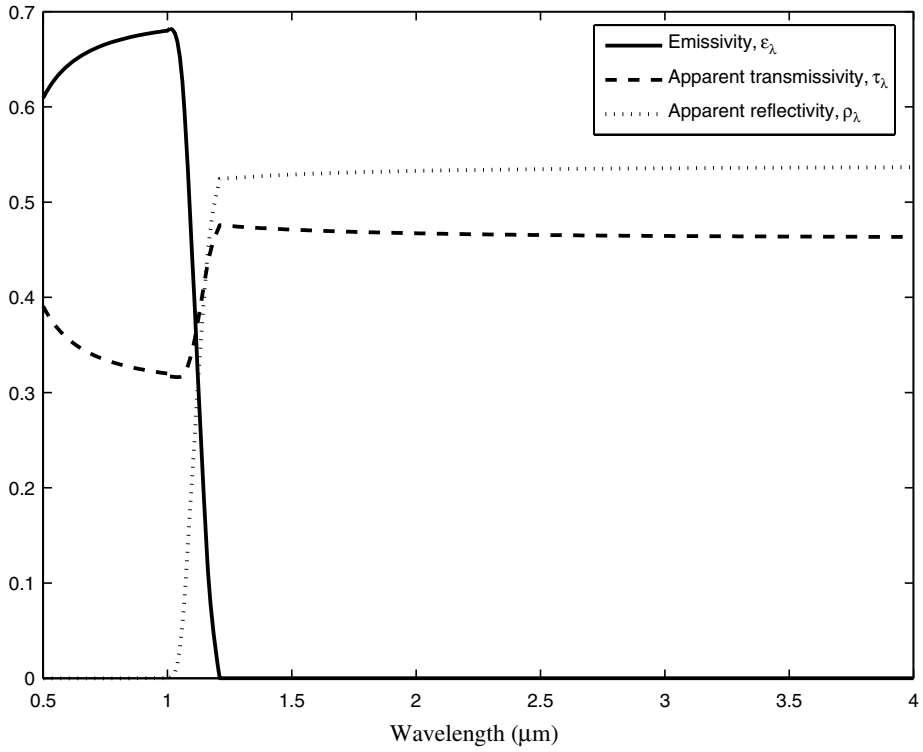

Fig. 2. Spectral emissivity, apparent transmissivity and apparent reflectivity of a silicon wafer at a temperature of 373 K. The wafer is 300 mm in radius and 675 μm thick.

For the wavelength range of interest, the radiation emitted by wafer element, i, denoted by q_i^{em} is given by

$$q_i^{\text{em}} = -\int_i \int_{0.5}^{4} \varepsilon_\lambda \frac{C_1 \lambda^{-5}}{\exp\left(\frac{C_2}{\lambda T}\right) - 1} \, \mathrm{d}\lambda \, \mathrm{d}A_i \tag{7}$$

where $C_1 = 3.7403 \times 10^8$ W μm^4/m^2 and $C_2 = 1.4387 \times 10^4$ μm K.

(2) Radiation absorbed by wafer element i, q_i^{abs}:

The main sources of radiative energy in the proposed system with which the wafer elements interact are the lamps and gold-coated chamber. For this purpose, the whole system is divided into $N = 77$ zones. The radiation absorbed by element i of the wafer can be expressed as follows

$$q_i^{\text{abs}} = \int_{0.5}^{4} (1 - \rho_\lambda - \tau_\lambda) \sum_{j=1, j\neq i}^{N} F_{ji} A_j J_{j,\lambda} \, \mathrm{d}\lambda \tag{8}$$

where $J_{j,\lambda}$, A_j and F_{ji} are respectively the spectral radiosity between zone j and element i, the surface area of zone j and the view factor [26] between each zone. The view-factor model used here is adapted from those of Norman [26] and Lord [32] which exhibit good agreement between simulation results and experimental data [32,33].

The spectral radiosity of each surface element i is denoted as $J_{i,\lambda}$ and given by

$$\begin{aligned}
J_{\text{lamp},i,\lambda}(t) &= \epsilon_{\text{lamp},\lambda} E_{\text{b},\lambda}\big(T_{\text{lamp}}(t)\big) \\
&\quad + \rho_{\text{lamp},\lambda} \frac{1}{A_{\text{lamp}}} \sum_{j=1}^{N} F_{ji} A_j J_{j,\lambda} \\
J_{\text{gold},i,\lambda}(t) &= \epsilon_{\text{gold},\lambda} E_{\text{b},\lambda}(T_{\text{gold}}(t)) \\
&\quad + \rho_{\text{gold},\lambda} \frac{1}{A_{\text{gold}}} \sum_{j=1}^{N} F_{ji} A_j J_{j,\lambda} \\
J_{\text{wafer},i,\lambda}(t) &= \epsilon_{\text{wafer},\lambda} E_{\text{b},\lambda}(T_{\text{wafer}}(t)) \\
&\quad + \rho_{\text{wafer},\lambda} \frac{1}{A_{\text{wafer}}} \sum_{j\neq \text{wafer,TED}}^{N} F_{ji} A_j J_{j,\lambda} \\
J_{\text{TED},i,\lambda}(t) &= \tau_{\text{w},\lambda} \Bigg[\epsilon_{\text{TED},\lambda} E_{\text{b},\lambda}(T_{\text{TED}}(t)) \\
&\quad + \rho_{\text{TED},\lambda} \tau_{\text{wafer},\lambda} \frac{1}{A_{\text{TED}}} \sum_{j\neq \text{wafer,TED}}^{N} F_{ji} A_j J_{j,\lambda} \Bigg]
\end{aligned}$$

where $E_{\text{b},\lambda}(T(t))$ is the spectral blackbody emission which is a function of temperature.

There are a total of N discrete surfaces with N linear equations. At every time instant, these surface radiosities can be computed algebraically and Eq. (8) computed accordingly.

(3) Conductive heat transfer from the TEDs into wafer element i, q_i^{cond}:

The air gap between the wafer and TEDs is 5 mils. Since this gap is much less than 5.8 mm, and their temperature difference considerably smaller than 200 °C [34], the heat transfer mechanism is essentially conductive and given by

$$q_z^{\text{cond}} = -kA_z \frac{\partial T}{\partial z} \tag{9}$$

where A_z is the cross-sectional area between wafer element i and the corresponding air gap.

The governing thermal equation for the air gap is given by

$$\rho c_p V_i \frac{\mathrm{d}T_{i,\text{air}}}{\mathrm{d}t} = \frac{k}{r} V_i \frac{\partial}{\partial r}\left(r \frac{\partial T_{i,\text{air}}}{\partial r}\right) + \frac{T_{\text{cera},i} - T_{i,\text{air}}}{L_{\text{cera}}/(2k_{\text{cera}}A_i) + L_{\text{air}}/(2k_{\text{air}}A_i)} + \frac{T_{\text{wafer},i} - T_{i,\text{air}}}{L_{\text{wafer}}/(2k_{\text{wafer}}A_i) + L_{\text{air}}/(2k_{\text{air}}A_i)} \tag{10}$$

with the following boundary conditions

$$\left.\frac{\partial T_{i,\text{air}}}{\partial r}\right|_{r=0} = 0$$

$$-k\left.\frac{\partial T_{i,\text{air}}}{\partial r}\right|_{r=D/2} = h(T_{i,\text{air}} - T_\infty)$$

(4) Convective heat transfer into wafer element i, q_i^{conv}:

The convective heat transfer between each element i of the wafer and the surrounding air is given by

$$q_i^{\text{conv}} = -h_i A_i (T_i - T_{\text{air}}) \tag{11}$$

where h_i is the area-weighted average convective heat transfer coefficient over the exposed surface area A_i of element i.

Heat is also transferred from the chamber to the air by convection. The equation for the convection term $q_{\text{cham}}^{\text{conv}}$ is given by

$$q_{\text{cham}}^{\text{conv}} = hA_{\text{cham}}(T_{\text{cham}} - T_{\text{air}}) \tag{12}$$

where A_{cham} is the internal surface of the chamber in contact with the air.

We note that in most practical radiative systems, some surfaces reflect specularly and others reflect diffusely. A rigorous calculation of the radiative heat transfer in the system demands the use of ray-tracing techniques [35], and entails a large programming effort as well as computing effort. Nevertheless, the present formalism has been found to yield good agreements with experimental data [32,33].

3.4. Thermoelectric devices (TEDs) modeling

The Peltier, Seebeck, Thomson and Joulean effects are the governing principles of thermoelectricity. For bismuth telluride, the Thomson effect is negligible [30]. Consequently the governing thermal transport equation in the semiconductor arms is given by [31]

$$\rho_{\text{t}} c_{p,\text{t}} \frac{\partial T_{\text{t}}}{\partial t} = k_{\text{t}} \frac{\partial^2 T_{\text{t}}}{\partial z_{\text{t}}^2} + \frac{J^2}{\sigma_{\text{t}}} \tag{13}$$

where $J(=I/A)$ the current flux where I and A are respectively the direct current flowing through the TEDs and the cross-sectional area. The subscript, t, denotes the thermoelectric modules.

Due to the choice of different materials for the metalization and for the thermoelectric arms, the Peltier effect is manifested at the boundary between the TED's metal contacts and the thermoelectric elements. It is given by

$$k_{\text{t}} A_{\text{t}} \frac{\partial T_{\text{t}}}{\partial z_{\text{t}}} + k_{\text{m}} A_{\text{m}} \frac{\partial T_{\text{m}}}{\partial z_{\text{m}}} \pm \alpha I T_{\text{b}} = 0 \tag{14}$$

The first two terms denote the thermal conduction into the interfacial layer while the last term represents the Peltier effect at the boundary. The sign in the last term in Eq. (14) is positive during heating mode and negative during chilling mode. During the heating mode, heat is generated at the interface which is then conducted away into both the metal contact and the thermoelectric arm, whereas during the cooling mode, heat is absorbed at the interface via conduction from both the metal contact and the thermoelectric arm. The thermal transport phenomenon in the metal film element is similarly expressed as

$$\rho_{\text{m}} c_{p,\text{m}} \frac{\partial T_{\text{m}}}{\partial t} = k_{\text{m}} \frac{\partial^2 T_{\text{m}}}{\partial z_{\text{m}}^2} + \frac{J^2}{\sigma_{\text{m}}} \tag{15}$$

The metal film is sandwiched between the thermoelectric elements and the ceramic substrates. Perfect contacts are assumed for all the interfaces. The equation describing the interface between the metal film and ceramic substrate is expressed as

$$-k_{\text{m}} A_{\text{m}} \left.\frac{\partial T_{\text{m}}}{\partial z_{\text{m}}}\right|_{\text{boundary}} = -k_{\text{ce}} A_{\text{ce}} \left.\frac{\partial T_{\text{ce}}}{\partial z_{\text{ce}}}\right|_{\text{boundary}} \tag{16}$$

The governing thermal transport equation of the ceramic substrate is

$$\rho_{\text{ce}} c_{p,\text{ce}} \frac{\partial T_{\text{ce}}}{\partial t} = k_{\text{ce}} \frac{\partial^2 T_{\text{ce}}}{\partial z_{\text{ce}}^2} \tag{17}$$

Additional boundary conditions are required for (i) the interface between the ceramic substrate and the chiller and (ii) the top ceramic plate facing the air-gap:

$$-k_{\text{ce}} A_{\text{ce}} \left.\frac{\partial T_{\text{ce}}}{\partial z_{\text{ce}}}\right|_{\text{boundary}} = -k_{\text{cop1}} A_{\text{cop1}} \left.\frac{\partial T_{\text{cop1}}}{\partial x_{\text{cop1}}}\right|_{\text{boundary}} \tag{18}$$

$$-k_{\text{ce}} A_{\text{ce}} \left.\frac{\partial T_{\text{ce}}}{\partial z_{\text{ce}}}\right|_{\text{boundary}} = \frac{T_{\text{ce,b}} - T_{i,\text{air}}}{R_{\text{a}}} + J_{\text{TED},\lambda}(t) - \tau_{\text{wafer},\lambda} G_{i\neq\text{wafer,TED}} \tag{19}$$

$G_{i\neq\text{wafer, TED}}$ denotes the irradiation of element i. R_{a} is the thermal resistance between the air gap and ceramic substrate element.

Finally, to compute the power consumption by each TED zone, consider the simplified schematic of a TED in Fig. 3. The electricity power consumed by each TED zone can be computed via an energy balance as

$$P_{\text{electricity}} = [P_{\text{out}} - P_{\text{in}} + \Delta P + 2\alpha \times I \times (T_{\text{b1}} - T_{\text{b2}})]N \tag{20}$$

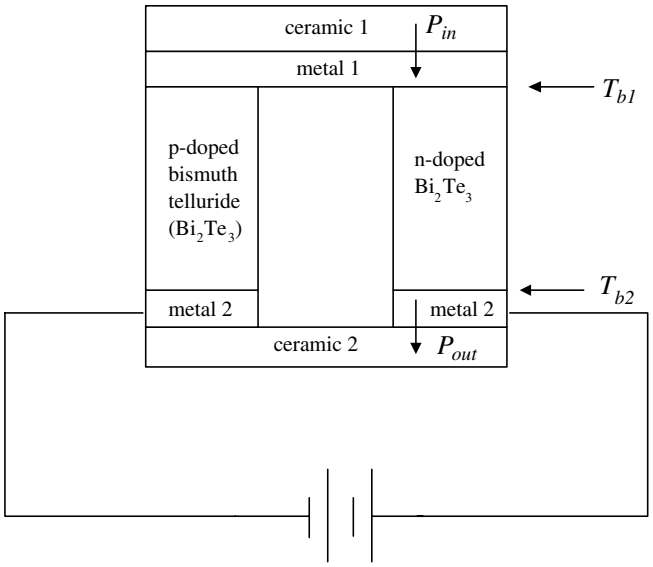

Fig. 3. Schematic diagram of a TED element. (*Note:* Figure not drawn to scale.)

where $P_{\text{out}} = -k_{\text{m}} A_{\text{m}} \frac{\partial T_{\text{m2}}}{\partial z_{\text{m2}}}$ is the energy transferred from metal 2 to ceramic 2; $P_{\text{in}} = -k_{\text{ce}} A_{\text{ce}} \frac{\partial T_{\text{ce1}}}{\partial z_{\text{ce1}}}$ the energy transferred from ceramic 1 to metal 1; $\Delta P = \sum \int_V \rho_i v_i c_{p,i} \frac{\partial T_i}{\partial t} \, \mathrm{d}V$ the internal power change, i stands for metal 1, metal 2 or TED; N is the number of pairs of TED arms in a particular zone; I the TED current and T_{b1}, T_{b2} are the respective metal–ceramic boundary temperatures.

3.5. Design of water chiller

During the cooling process, heat absorbed at the cold junction of TEDs is pumped to the hot junction. At the hot junction, the energy absorbed is dissipated via the chiller. Fig. 1(c) shows the schematic of the water chiller. The chiller is made of copper. The top layer is 3 mm thick while the bottom layer is made thicker at 6 mm in order to accommodate a tunnel inside to facilitate circulation of water. The dimension of the cross section of water vessel is 20 mm × 20 mm. The counterflow Archimedes' spiral design for the copper based chiller effectively ensures spatial temperature homogeneity throughout the region which is in contact with the TED array. Note that the incoming chilled water converges at the center of the spiral heat exchanger which then spirally radiates out again via the adjoining outgoing channel; also referring to Fig. 1(c) the chiller has been deliberately oversized to weed out any end effects on the TED array.

To provide efficient heat dissipation, turbulent water flow inside chiller has to be maintained which requires

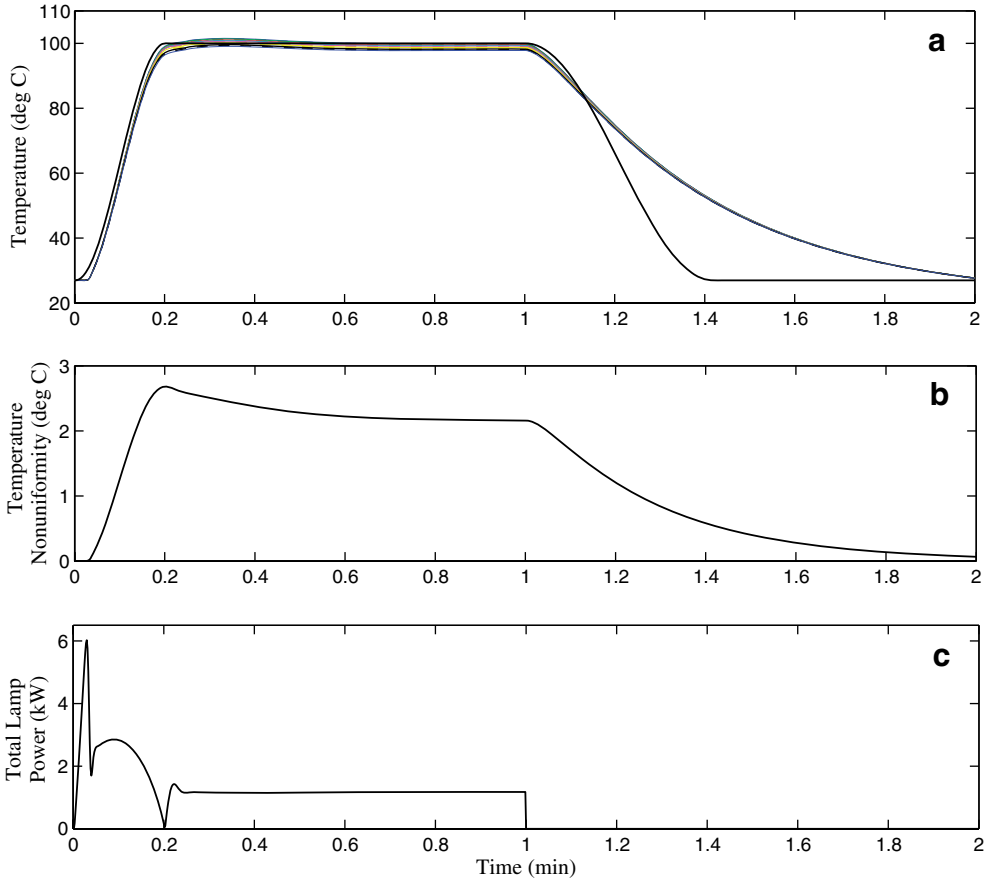

Fig. 4. Wafer temperature responses at 15 measurement sites along the radius of the wafer during a thermal cycle. The system is set up as a single zone system with the center of the wafer temperature being fed back to the controller. The second plot shows the maximum temperature nonuniformity between the different zones during the entire thermal cycle. The third plot shows the total lamp power.

the Reynolds number to be always higher than 3000 in the simulation. An initial water flow rate 0.15 kg/s is accordingly applied which corresponds to a Reynolds number of 7500. The energy balance equation of the chiller is given as

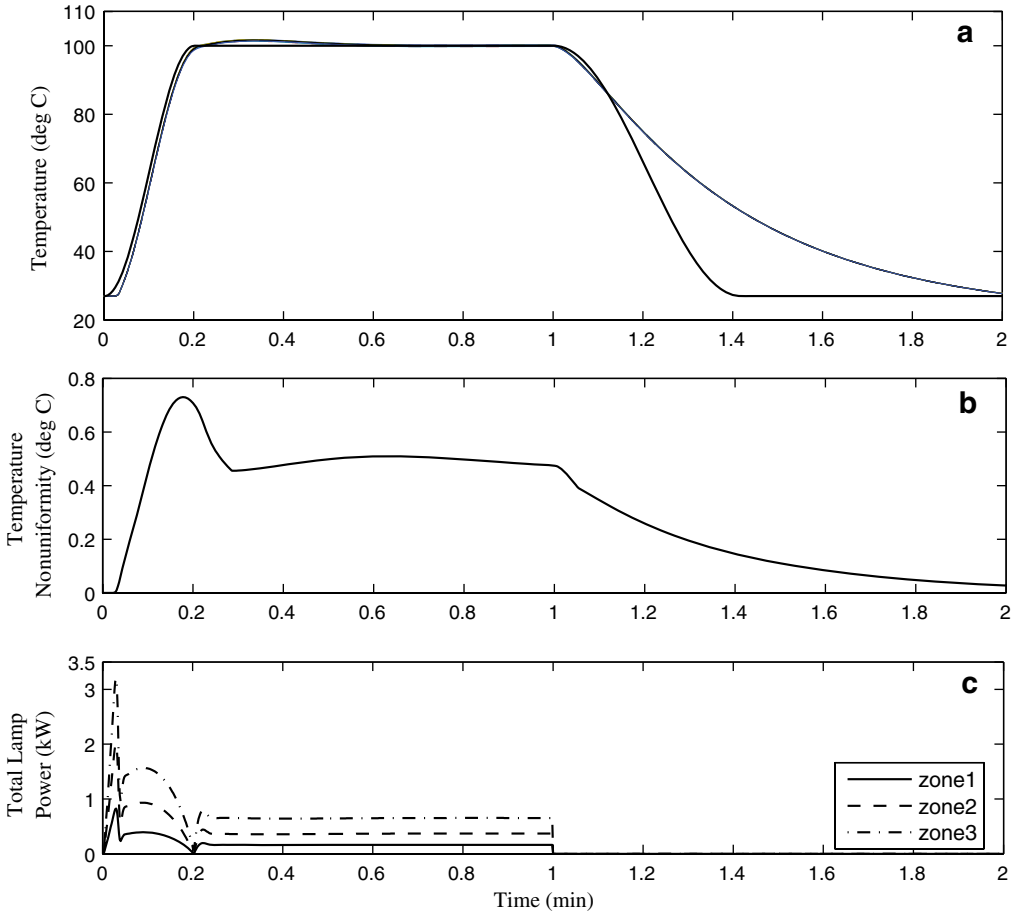

Fig. 5. Wafer temperature responses at 15 measurement sites along the radius of the wafer during a thermal cycle. The system is set up as 3 single decentralized systems with each of the wafer temperatures directly below each of the lamp locations being fed back to the respective lamp controllers. The second plot shows the maximum temperature nonuniformity between the different zones during the entire thermal cycle. The third plot shows the lamp power in each of the lamp zones. Solid line indicates the innermost zone, dashed line indicates the middle zone and dotted line indicates the outermost zone.

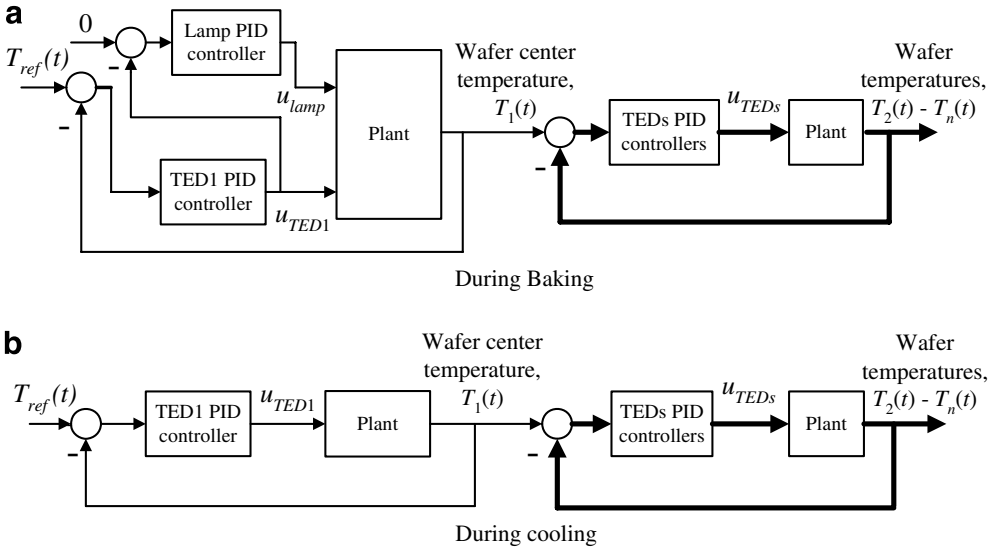

Fig. 6. Block diagram of the integrated bake/chill control configuration.

$$c_{p,\mathrm{chi}} m_{\mathrm{chi}} \frac{\mathrm{d}T_{\mathrm{chi}}}{\mathrm{d}t} = hA(T_{\mathrm{cop1}} - T_{\mathrm{chi}}) + hA(T_{\mathrm{cop2}} - T_{\mathrm{chi}}) - \dot{m} c_{p,\mathrm{water}} (T_{\mathrm{chi}} - T_{\mathrm{in,water}}) \quad (21)$$

where $\dot{m}$ the mass flow rate of the cooling water; $T_{\mathrm{in,water}} = 20\ ^\circ\mathrm{C}$ is the temperature of water at the inlet of the chiller and the convective heat coefficient, h, can be calculated from [36]

$$f = (0.79\ln(Re) - 1.64)^{-2}$$
$$Nu = \frac{(f/8)(Re - 1000)Pr}{1 + 1.27(f/8)^{1/2}(Pr^{2/3} - 1)}$$

A standard proportional–integral–derivative (PID) controller is used to control the chiller flow rate so as to maintain the chiller temperature at a desired level. For our simulation, the chiller setpoint is set equal to the water temperature at the inlet of the chiller. The PID controller is of the following form

$$u(t) = K_{ci}\left(e(t) + \frac{1}{T_{Ii}}\int e(t)\,\mathrm{d}t + T_{di}\frac{\mathrm{d}e(t)}{\mathrm{d}t}\right) \quad (22)$$

where K_{ci}, T_{Ii} and T_{di} are the controller parameters; $u(t)$ and $e(t)$ are respectively the control signal to the valve controlling the water flow rate and the error between the desired and actual water temperatures.

4. Control and simulation results

Simulations were carried out to assess the performance of the proposed lamp-TEDs thermal processing system. Our objective is to demonstrate that the proposed design is able to maintain temperature uniformity during the entire thermal cycling process. We will demonstrate that because of the decoupled nature of the system design, simple decentralized controllers can be used for this system without going into more advanced multivariable controllers. The lamps will be used to provide the bulk heating while the TEDs are used to address the non-uniformity problem between the different zones. During chilling, the lamps are turned off and the TEDs are used to minimize the temperature non-uniformity. For simplicity, the lamp portion of the system is treated as a single input system, i.e., one control signal is sent to the three zones of lamps.

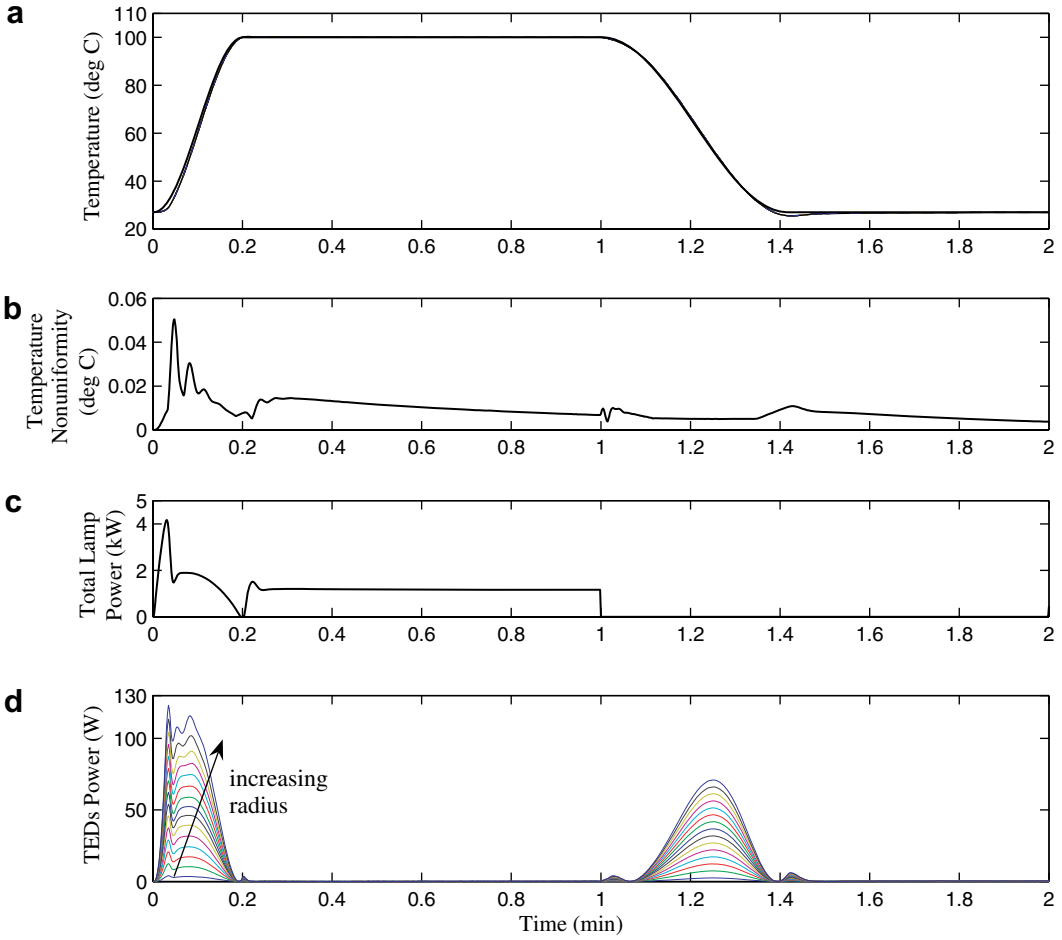

Fig. 7. Wafer temperature responses at 15 measurement sites along the radius of the wafer during a thermal cycle. The second plot shows the maximum temperature nonuniformity between the different zones during the entire thermal cycle. The third plot shows the total lamp power. The TED power in each of the zones is shown in the bottom plot.

Table 1 shows the thermophysical properties of the parameters [31,37] used in the simulation.

In the simulation, two sets of temperature are of interest, namely the real and measured temperatures of the wafer. The sensor model is given as

$$\frac{dT_{\text{measured}}}{dt} = \frac{1}{\tau}(T_{\text{real}} - T_{\text{measured}}) \tag{23}$$

where τ is the time constant of the temperature sensor; for the temperature sensors modeled, $\tau = 25$ ms. For the simulation, a sampling time of 0.1 s is used. As expected, the measured temperature is a slightly delayed response to temperature variations due to the sensor dynamics.

We first analyze the capability of the lamp system without the TEDs. Fig. 4 shows the wafer temperature responses at 15 equally spaced measurement sites along the radius of a 300 mm wafer during a thermal cycle. The feedback system is set up with a simple PID controller where the feedback temperature stems from the center of the wafer. The same control signal generated by the PID controller is sent to the three different lamp zones. It is thus a single-input-single-output system design [13]. Notice that the peak temperature non-uniformity is about 2.7 °C during the transient period; a slight improvement could be obtained by feeding back other spatial wafer temperature points. An alternative and improved control approach is to make use of the multizone nature of the lamp system. Since the lamp system consists of three zones, three wafer temperature measurements directly below each of the lamp locations provide feedback to the respective lamp controllers. Fig. 5 demonstrates the temperature response of the 3-zone setup. Notice that the peak temperature non-uniformity has dropped to about 0.7 °C. Again other wafer temperature locations can be chosen for feedback, however the improvement is limited.

We now investigate the use of the TEDs to regulate and improve the spatial temperature uniformity. Closed-loop control using the 15-zone system was configured as shown in Fig. 6 where the block plant represents the thermal processing system. The innermost zone causes the wafer center temperature to follow a desired wafer temperature trajectory. The rest of the zones maintains temperature uniformity by forcing their temperatures to follow the wafer center temperature. The individual controllers used are of the PID type; in short, a decentralized control scheme is used [13]. During baking, a cascade control structure is used as shown in Fig. 6(a). The cascade implementation [13] has the advantages of decoupling the design of the lamp and TED controllers where u_{TED1} takes care of the fast control and u_{lamp} the long-term control. Note that a single-zone lamp configuration is used here, our simulation shows that this is sufficient to obtain the desired specifications.

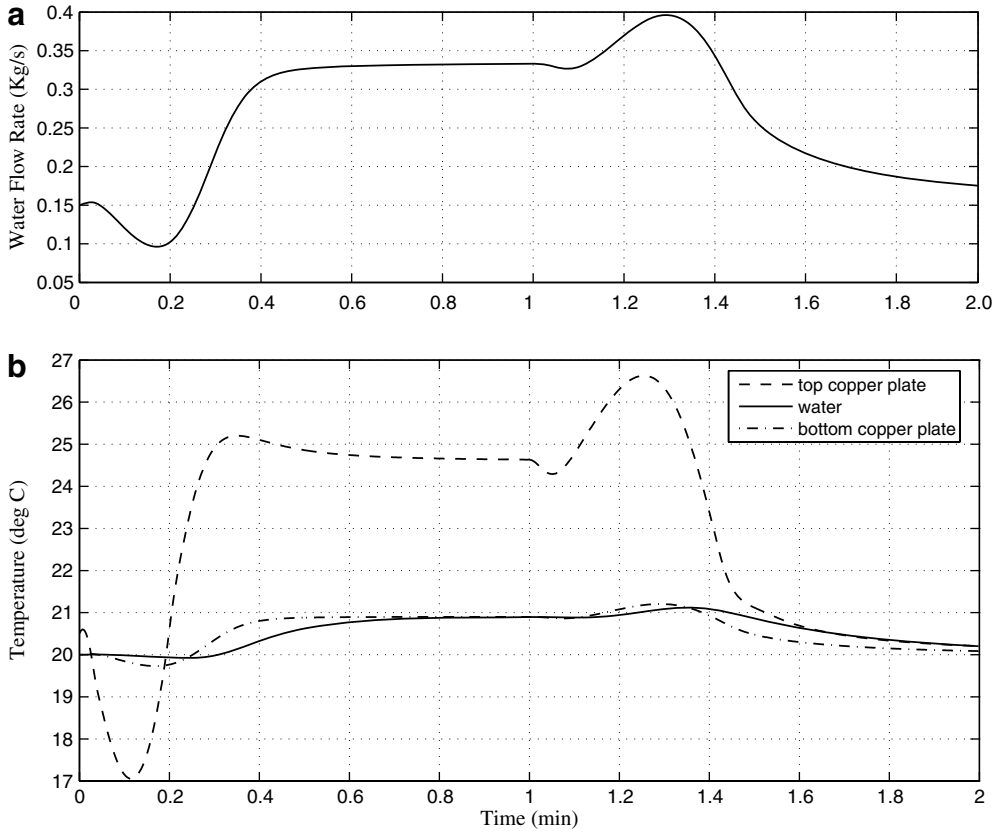

Fig. 8. Flow rate and chiller temperature responses during the entire thermal cycle.

Fig. 7 shows the wafer temperature responses. The temperature non-uniformity is less than 0.1 °C during the entire thermal cycle. The rise time of 10 s is much faster than conventional proximity bake systems which typically have a rise time of about 20–30 s [10]. This is made possible due to the lamp based heating approach. The total lamp power is also shown in Fig. 7; as expected, the power consumption is high during the initial transient period. The electrical powers to the 15 zones of TEDs during a thermal cycle are shown in the bottom plot. Since the lamp configuration is designed

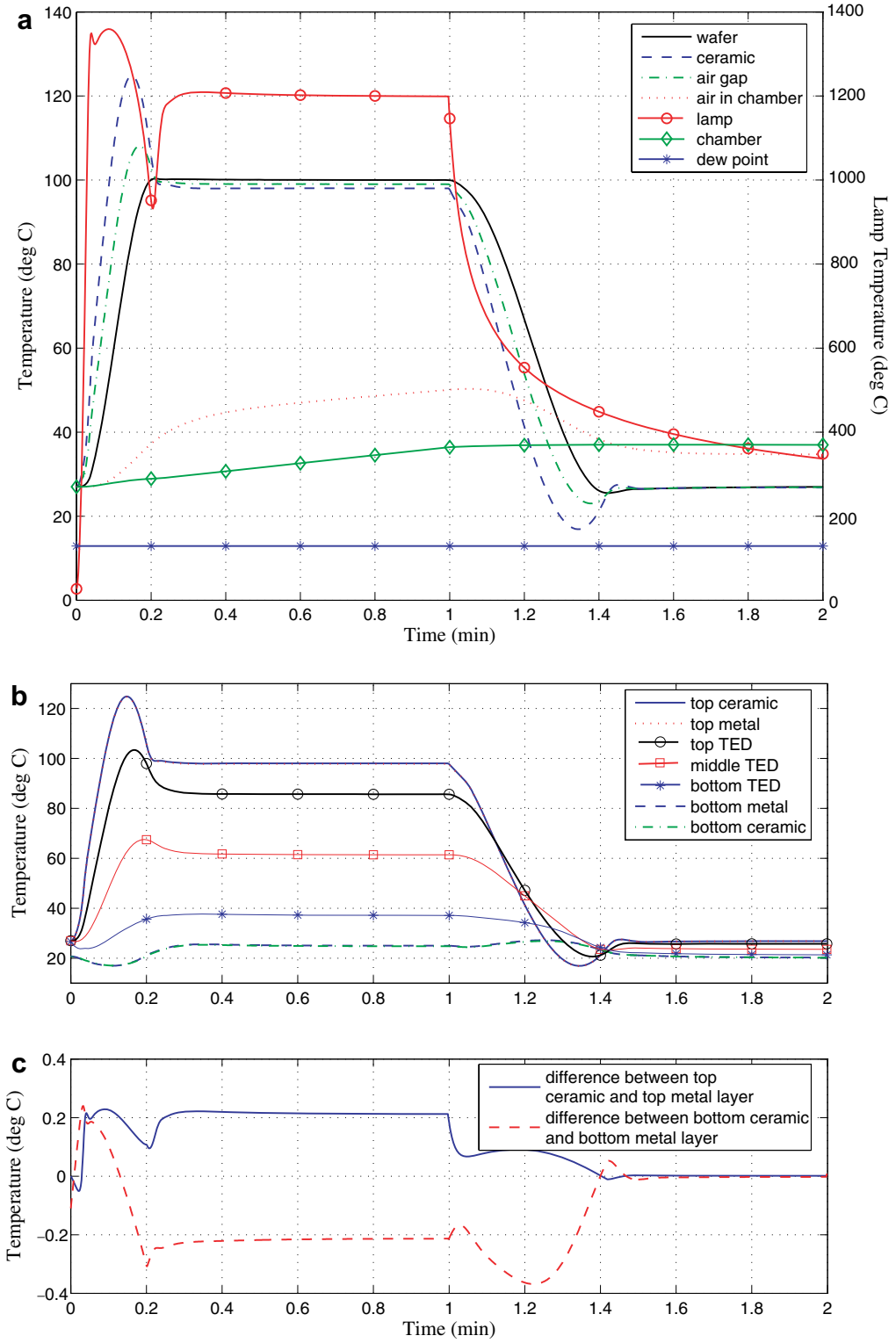

Fig. 9. Different surface temperature during the entire thermal cycle shown in Fig. 7. The lamp temperature is indicated on the right ordinate. Temperatures of different layers of TEDs during an entire thermal cycle shown in (b) and (c).

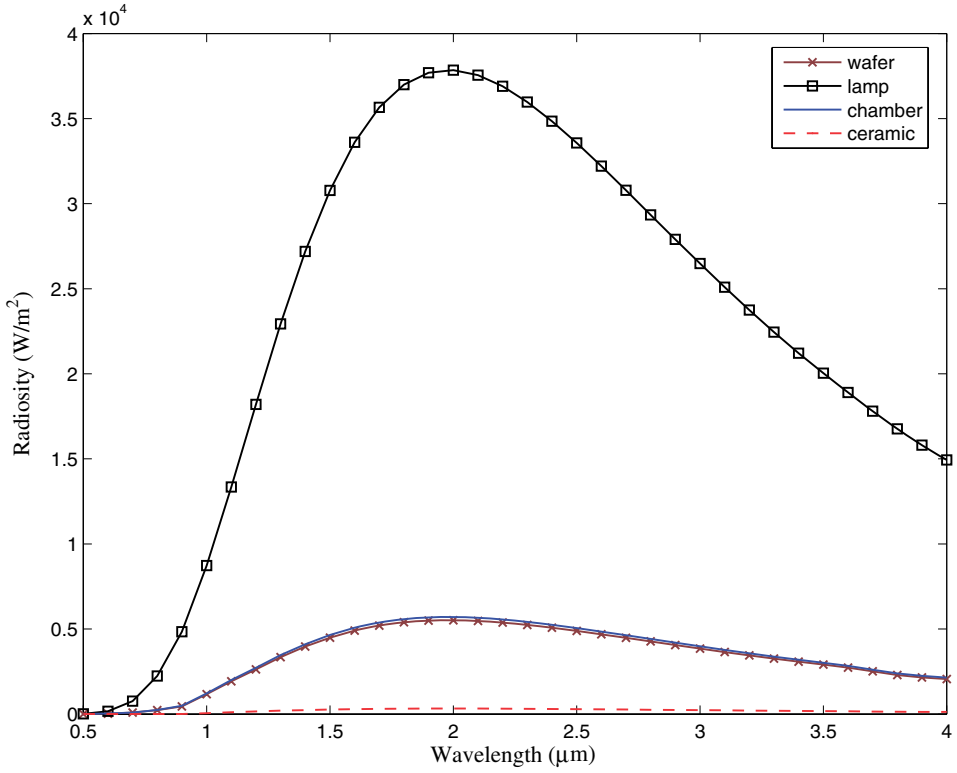

Fig. 10. Spectral radiosities for the different surfaces at the tenth second of the thermal cycle shown in Fig. 7.

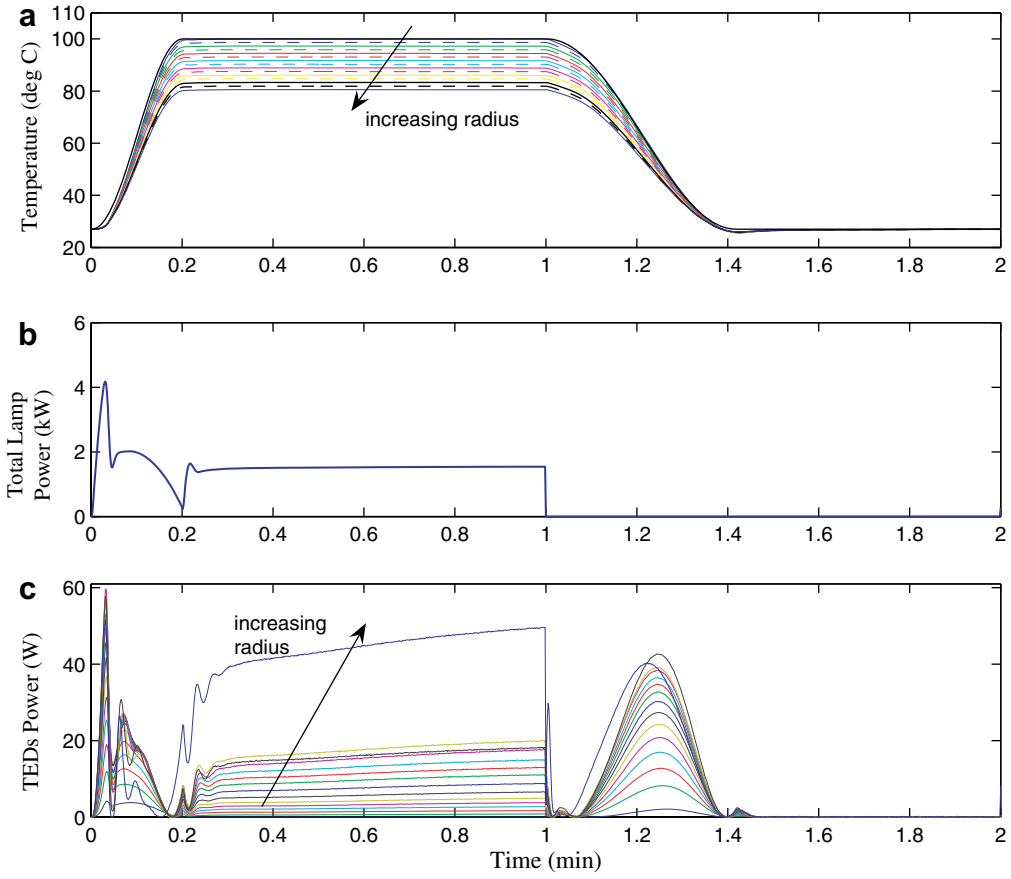

Fig. 11. Wafer temperature responses at 15 measurement sites along the radius of the wafer during a thermal cycle with temperature biasing. Each zone is set to a different temperature trajectory with a temperature difference of 1.4 °C between each zone at steady state. The lamp and TEDs power are also shown.

to achieve tight temperature uniformity, any temperature regulation during the baking process from the TEDs is minimal as shown in Fig. 7(d). Notice that the zone powers are neither equal nor proportional in magnitude. In fact the different zones have very different power distribution to achieve temperature uniformity thereby demonstrating the power of the proposed multizone approach. We note also that better temperature uniformity could be achieved by retuning the respective controllers, a more powerful approach is to design a multivariable controller that takes into account the interaction between each zone [13]. Fig. 8 shows the flow rate of the chiller and its corresponding temperature. The temperature of the chiller is regulated back to its original temperature after each wafer run so that the process is repeatable for each processing cycle.

Fig. 9(a) shows the respective surface temperature during the thermal cycle. The wafer and TEDs (ceramic) surfaces are obtained from the center of the wafer. The lamp and chamber is assumed to be isothermal and hence represented by a single temperature respectively. As expected, the ceramic surface is at a higher temperature compared to the wafer during initial transient baking and lower temperature during the initial transient chilling. During the chilling process, the lowest temperature of the ceramic surface is about 17 °C. In a typical cleanroom environment, the air temperature is about 24 °C and with a the relative humidity of about 50%, the dew-point temperature is about 13 °C. Since the temperature of the top ceramic is considerably higher than the dew-point temperature, we can rule out the chances of condensation during thermal cyclings. The temperature of the different TED layers are shown in Fig. 9(b) and (c). Fig. 10 shows the corresponding radiosities of the various surfaces.

In determining the recipes for post-exposure baking, it is normally necessary to obtain data at multiple temperatures. These studies can be time-consuming and costly. In addition, errors can occur if drifts in the other equipment affect results and thus making it difficult to determine the impact the temperature has on the process. Using the proposed system, it becomes possible however to achieve several different processing temperatures using a single experiment. This situation is achieved by programming the temperature to different set points across the surface of the substrate by utilizing the multizone temperature control capability. Fig. 11 shows the 15 zones on the substrate can be controlled such that the temperature set point for each zone is separated by 1.4 °C. Other distributions of temperature are certainly possible, where each temperature site across the entire substrate is biased. This capability also demonstrates the decoupled nature of the system.

5. Conclusions

We have presented the design of an integrated bake/chill module for photoresist processing in microlithography and assessed the feasibility of the proposed approach based on a detailed modeling approach. Our proposed thermal system consists of multiple radiant heating zones achieved with tungsten halogen lamps for heating the substrate. This is coupled with an array of thermoelectric devices (TEDs) which provide real-time dynamic and spatial control of the substrate temperature. The TEDs also provide active cooling for chilling the substrate to a temperature suitable for subsequent processing steps. Our radiant heating feature offers fast ramp-up and ramp-down rates during thermal cycling operations. The distributed nature of the design also engenders a simple decentralized control scheme which satisfies tight spatial and temporal temperature uniformity specifications. Transient and steady-state temperature uniformity of less than 0.1 °C can be achieved.

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